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EXAMINER	
ROSALES HANNER, MORELLA I	
ART UNIT	**PAPER NUMBER**
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/631,427	STEVEN P. LARKY	
	Examiner	Art Unit	
	Morella I Rosales-Hanner	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 0200*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1 - 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 0200* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 1 – 20 are pending and have been examined.

Drawings

2. The drawings are objected to because they fail to comply with 37 CFR 1.84(p) (refer to form PTO-948). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The specification is objected to for the following reason: the specification refers to the element **[page 9, line 11] system 50**, which doesn't appear to be in either two of the submitted drawings. It appears that this should be **system 100**. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4 The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4.1 Claims 1 – 20 are rejected under 35 U.S.C. 112, first paragraph, because of the following informalities: applicant use of the word '**may**' in multiple places while describing the invention renders the disclosure inadequate. One of ordinary skills in the art would not be able to make and use the intended invention. For Example, the application recites **[pg 8, lines 1 - 4]**:

"appropriate attributes and/or parameters may include applicable digital and/or analog parameters"

It is unclear what the attributes include. The specification is full with such deficiencies. Appropriate correction is required without adding new matter.

4.2 **Claims 1 – 20** are rejected under 35 U.S.C. 112, first paragraph, as failing to provide adequate written description of the intended invention. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. For example, **claim 1** recites:

"A method for modeling analog signals comprising the steps of:

(A) **detecting** one or more attributed analog signals; and
(B) **modeling** said attributed analog signals by adding a signature to each of said one or more attributed signals. "

The specification fails to disclose:

- how the attributed analog signals are detected or
- how the attributed analog signals are modeled.

Furthermore, **claim 20** **[lines 3 – 10]** recites:

"adding a **first signature** to at least one of said one or more attributed analog signals; and adding a **second signature** to said at least one attributed

analog signal, wherein said **first signature** corresponds to a **first predetermined** parameter of said one or more predetermined parameters and said **second signature** corresponds to a **second predetermined** parameter of said one or more predetermined parameters."

The specification fails to disclose adding a second signature.

In Keeping with the practice of compact prosecution, the following rejection is advanced against the claims as best interpreted.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5.1 **Claims 1 – 9, 11 – 14, and 17 - 19** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by a printed publication by Sassan Tabatabaei and Andre Ivanov, titled "A Built-in Current Monitor for Testing Analog Circuit Blocks" dated May 1999, hereafter referred to as *Tabatabaei*

5.1.1 As regard to Independent **claim 1,** this claim is drawn to modeling analog signals by:

- detecting attributed analog signals and

- modeling attributed analog signals by adding a signature

Per independent **claim 1**: *Tabatabaei* discloses modeling analog signals **[Pg II-110, section 1.3]** by detecting (sensing) **[Pg II-110, section 1.3, line 2]** analog signals. *Tabatabaei* further discloses **[Pg II-110, section 1.3, line 12]** a current integrator circuit, which generates and integrates a digital signature to the analog signal.

5.1.2 As regard to independent **claim 9**, this claim is drawn to testing a model of a device by:

- performing tests on the model of a device; and
- verifying connectivity of attributed analog signals within the model by verifying their signatures.

Tabatabaei teaches **[Pg II-113, section 3, paragraph 1]** the use of BSIM1 MOS models to perform simulations of a Built-in Current (**BIC**) monitor circuit for analog and mixed-signal simulations. *Tabatabaei* also teaches **[Pg II-110, section 1.3, paragraph 3]** a built-in current integrator (**BICI**) block, which is part of a **BIC** monitor circuit, that generates a digital signature proportional to the average supply current I_{DD} and is suitable for Built-in Self Test (**BIST**) applications since it generates a digital signature which can be easily evaluated (verified) on chip by simple digital circuitry.

5.1.3 As regard to dependent **claim 2**, this claim is drawn to performing digital simulations with analog signals.

Tabatabaei discloses **[Pg II-113, section 3, line 5]** simulation results for analog signal simulation for a set of 13 different current signals with different waveforms, frequencies, amplitudes and offset values.

5.1.4 As regard to dependent **claim 3**, this claim is drawn to a signature that correspond to a predetermined parameter.

Tabatabaei discloses **[Pg II-113, section 3, line 5]** simulation using thirteen different analog signals with different parameters such as waveforms, frequencies, amplitudes and offset values to test the BICI's that generates a digital signature proportional to the analog signal.

5.1.5 As regard to dependent **claim 4**, this claim is drawn to modeling analog signals by:

- detecting attributed analog signals and
- modeling attributed analog signals by adding a digital signature.

Tabatabaei discloses modeling analog signals **[Pg II-110, section 1.3]** by detecting (sensing) **[Pg II-110, section 1.3, line 2]** analog signals. *Tabatabaei* further discloses **[Pg II-110, section 1.3, line 12]** a current integrator circuit, which generates and integrates a digital signature to the signal.

5.1.6 Dependent **claim 5** is drawn to performing verification of the attributed analog signals (from claim 1).

Tabatabaei teaches [**Pg II-110, Fig. 1**] a built-in current monitor that has two main parts: a built-in current sensor (BICS) and a built-in current integrator (**BICI**). *Tabatabaei* further teaches [**Pg II-110, section 1.3, paragraph 3**] a BICI block that generates a digital signature proportional to the average supply current I_{DD} which is suitable for Built-in Self Test (**BIST**) applications since it generates a digital signature which can be easily evaluated (verified) on chip by simple digital circuitry.

5.1.7 Dependent **claim 6** is drawn to determining connectivity of an attributed signal (from claim 1).

Tabatabaei teaches [**pg II-114, Section 4**] the use of a built-in current monitor (**BIC**) [**Pg II-110, Fig. 1**] that can be used as a signature generator and is suitable for power supply current (I_{DD}) testing of analog circuit blocks.

5.1.8 Dependent **claims 7, 8, and 11** are drawn to verifying a model of an analog block configured to receive at least one of the attributed signals (from claim 1).

Tabatabaei teaches [**pg II-113, Section 3**] the use of Cadence SpectreS and SpectreSVerilog to perform simulations of the built-in current (BIC) monitor circuit [**Fig 1**]. *Tabatabaei* further teaches the use of BSIM1 MOS models for analog and mixed-signal simulations.

5.1.9 As regard to dependent **claim 12,** this claim is drawn to verifying a second one or more models of analog blocks configured to receive attributed analog signals.

Tabatabaei discloses [**Pg II-113, section 3**] the use of Cadence SpectreS and SpectreSVerilog to perform simulation of the built-in current monitor, use of BSIM1 MOS models for analog and mixed-signal simulations, and BICI circuit simulation testing (verification) using a set of 13 different current signals with different waveforms, frequencies, amplitudes and offset values.

5.1.10 As regard to **independent claim 13 and dependent claim 17, independent claim 13** is drawn to verifying a model of a device by:

- detecting attributed analog signals; and
- performing verification of predetermined parameters in response to the attributed analog signals.

Dependent **claim 17** is drawn to using analog parameters as predetermined parameters.

Tabatabaei discloses modeling analog signals [**Pg II-110, section 1.3**] by detecting (sensing) [**Pg II-110, section 1.3, line 2**] analog signals. *Tabatabaei* further discloses [**Pg II-113, section 3**] the use of BSIM1 MOS models for analog and mixed-signal simulations, and BICI circuit simulation testing (verification) using a set of 13 different current signals with different waveforms, frequencies, amplitudes parameters and offset values.

5.1.11 As regard to dependent **claim 14**, this claim is drawn to adding a signature to attributed analog signals.

Tabatabaei discloses [**Pg II-110, section 1.3, line 12**] a current integrator circuit, which generates and integrates a digital signature to analog signals.

5.1.12 As regard to dependent **claim 18**, this claim is drawn to determining connectivity of attributed analog signals.

Tabatabaei teaches [**Pg II-110, section 1.3, paragraph 3**] the use of a built-in current integrator (**BICI**) block that can be used to easily evaluate (verify) attributed analog signals and is suitable for Built-in Self Test (**BIST**) applications since it generates a digital signature which can be easily evaluated (verified) on chip by simple digital circuitry.

5.1.13 As regard to dependent **claim 19**, this claim is drawn to verifying a model of an analog block in response to attributed analog signals.

Tabatabaei [**Pg II-113, section 3**] the use of BSIM1 MOS models for analog and mixed-signal simulations, and BICI circuit simulation testing (verification) using a set of 13 different current signals with different waveforms, frequencies, amplitudes parameters and offset values.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.1 **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over a printed publication by Sassan Tabatabaei and Andre Ivanov, titled "**A Built-in Current Monitor for Testing Analog Circuit Blocks**" dated May 1999, hereafter referred to as *Tabatabaei* as applied to claim 9 above, and further in view of another printed publication by Sassan Tabatabaei and Andre Ivanov, titled "**A Current Integrator for BIST of Mixed-Signals IC's**" dated 1999, hereafter referred to as *Tabatabaei2*. **Claim 10** is drawn to disabling a device if one or more attributed analog signals are not verified.

Tabatabaei teaches **[Pg II-110, section 1.3, paragraph 3]** the use of a built-in current integrator (**BICI**) block that can be used to easily evaluate (verify) attributed analog signals and is suitable for Built-in Self Test (**BIST**) applications since it generates a digital signature which can be easily evaluated (verified) on chip by simple digital circuitry, as discussed above.

Tabatabaei fails to expressly teach disabling a device if its attributed analog signals are not verified.

Tabatabaei2 teaches **[Section 3, paragraph 1, lines 24 - 32]** discarding (disabling) a circuit if one or more of its attributed analog signals falls bellow a threshold and fails verification. *Tabatabaei2* also teaches **[section 1]** that testing of complex mixed

analog/digital circuits is still a hard and expensive task. *Tabatabaei2* further teaches that built-in self test (BIST) techniques are known to be efficient in reducing the test cost of a circuit because these techniques allow the transfer of some of the resources from automatic test equipment (ATE) into circuit under test (CUT). In particular, on-chip signature analysis consists in designing built-in devices to compress the output response, to an analog signal, into a signature, comparing this signature to a predetermined one and, generating a "go/no-go" signal.

For this reason, it would have been obvious to one of ordinary skills in the art, at the time of the invention, to modify the built-in device taught by *Tabatabaei* to compare the generated signature to a predetermined value in order to generate a "go/no-go" signal as taught by *Tabatabaei2*.

6.2 **Claims 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over a printed publication by Sassan Tabatabaei and Andre Ivanov, titled "**A Built-in Current Monitor for Testing Analog Circuit Blocks**" dated May 1999, hereafter referred to as *Tabatabaei* as applied to claim 13 above, in view of another printed publication by Franc Novak, Bojan Hvala and Sandi Klavzar, titled "**On Analog Signature Analysis**", dated 1999, hereafter referred to as *Novak et al.* Claim 15 is drawn to adding an unique digital signature to analog signals

Tabatabaei discloses **[Pg II-110, section 1.3, line 12]** a current integrator circuit, which generates and integrates a digital signature to analog signals, as discussed above.

Tabatabaei fails to expressly disclose adding a digital signature to attributed analog signals that is unique.

Novak et al. discloses **[Pg. 1, section1, paragraph 2]** that generation of unique signatures has proved to be an effective fault detection and localization technique for digital circuits. *Novak et al.* further discloses **[Pg. 1, Col. 2, paragraph 2]** the possibility of defining a unique signature in the analog domain that could be a suitable basis for automatic testing and diagnosing of analog circuits.

For this reason, it would have been obvious to one of ordinary skills in the art, at the time of the invention, to generate a digital signature for analog signals as disclosed by *Tabatabaei* that is unique as disclosed by *Novak et al.* in order to make it suitable for automatic testing and diagnosing of analog circuits.

6.3 **Claims 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over a printed publication by Sassan Tabatabaei and Andre Ivanov, titled "**A Built-in Current Monitor for Testing Analog Circuit Blocks**" dated May 1999, hereafter referred to as *Tabatabaei* as applied to claim 13 above, in view of another printed publication by Sassan Tabatabaei and Andre Ivanov, titled "**A Current Integrator for BIST of Mixed-Signals IC's**" dated 1999, hereafter referred to as *Tabatabaei2*, and in further view of a printed publication from Chen-Yang Pan and Kwang-Ting (Tim) Cheng, titled "**Pseudorandom Testing for Mixed-Signal Circuits**" dated 1997, hereafter referred to as *Pan et al.* This claim is drawn to using digital parameters as predetermined parameters while verifying a model of a device as claimed in **claim 13** (addressed in section 5.1.10 above).

Tabatabaei teaches **[Pg II-113, section 3, paragraph 2]** model simulations of a device using thirteen different analog signals with different parameters such as waveforms, frequencies, amplitudes and offset values. *Tabatabaei* teaches **[Pg II-109, section 1, paragraph 1]** that the success of supply current monitoring in digital CMOS integrated circuits has prompted researchers to investigate the use of this technique with analog signals. See above discussion.

Tabatabaei fails to expressly teach the use of digital predetermined parameters for verifying a model of a device.

Tabatabaei2 teaches **[section 3, paragraph 2]** the use of signals SPK1 and SPK2 **[Figs 8a and 8b]** used to model supply current of digital circuit blocks. *Tabatabaei2* also teaches **[section 1, paragraph 1]** that the success of supply current monitoring in digital CMOS integrated circuits has prompted researches to investigate the use of this technique with analog signals.

Pan et al. teaches **[Pg 1173, Col 1, paragraph 1]** that due to the different types of circuitry involve, it usually requires several completely different schemes to test a mixed-signal chip.

For this reason, it would have been obvious to one of ordinary skills in the art, at the time of the invention, to modify the model of a device as disclosed by *Tabatabaei* to use digital predetermined parameters during the simulation (test) of the device as disclosed by *Tabatabaei2* in order to take advantage of the success the supply current monitoring technique, as a testing methodology for digital circuits, has proven in order to

reduce the number of completely different schemes needed to test a mixed-signal chip as taught by *Pan et al.*

Conclusion

7. The examiner has determined that the specification for the claimed invention is delinquent in the areas cited under 112(1), and has therefore made prior art rejections based on the limited scope of information contained in the specification and a good faith interpretation of the language of the claims.

The examiner also rejects all claims under 102(b) and 103(a).

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Linda S. Milor, "**A tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing**", October 1998, IEEE Transactions on Circuits and Systems – II
- M. Renovell, F. Azais and Y. Bertrand, "**On-Chip Analog Output Response Compaction", 1997**, ED&TC '97 on CD-ROM

9. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Morella Rosales-Hanner whose telephone number is (703) 305-8883. The examiner can normally be reached Monday-Friday from 7:00 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MRH

Mar. 18, 2004